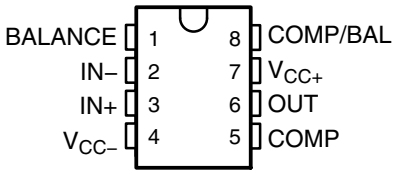
- **Equivalent Input Noise Voltage . . . 3.5 nV/√Hz Typ**
- **Unity-Gain Bandwidth . . . 10 MHz Typ**
- **Common-Mode Rejection Ratio . . . 100 dB Typ**
- **High DC Voltage Gain . . . 100 V/mV Typ**
- **Peak-to-Peak Output Voltage Swing 32 V Typ With $V_{CC\pm}$ = ±18 V and R_L = 600 Ω**
- **High Slew Rate . . . 13 V/μs Typ**
- **Wide Supply-Voltage Range ±3 V to ±20 V**
- **Low Harmonic Distortion**
- **Offset Nulling Capability**
- **External Compensation Capability**

NE5534, SA5534 . . . D (SOIC), P (PDIP), OR PS (SOP) PACKAGE
NE5534A, SA5534A . . . D (SOIC) OR P (PDIP) PACKAGE
(TOP VIEW)



description/ordering information

The NE5534, NE5534A, SA5534, and SA5534A are high-performance operational amplifiers combining excellent dc and ac characteristics. Some of the features include very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, and high slew rate.

These operational amplifiers are compensated internally for a gain equal to or greater than three. Optimization of the frequency response for various applications can be obtained by use of an external compensation capacitor between COMP and COMP/BAL. The devices feature input-protection diodes, output short-circuit protection, and offset-voltage nulling capability with use of the BALANCE and COMP/BAL pins (see the *application circuit* diagram).

For the NE5534A and SA5534A, a maximum limit is specified for the equivalent input noise voltage.

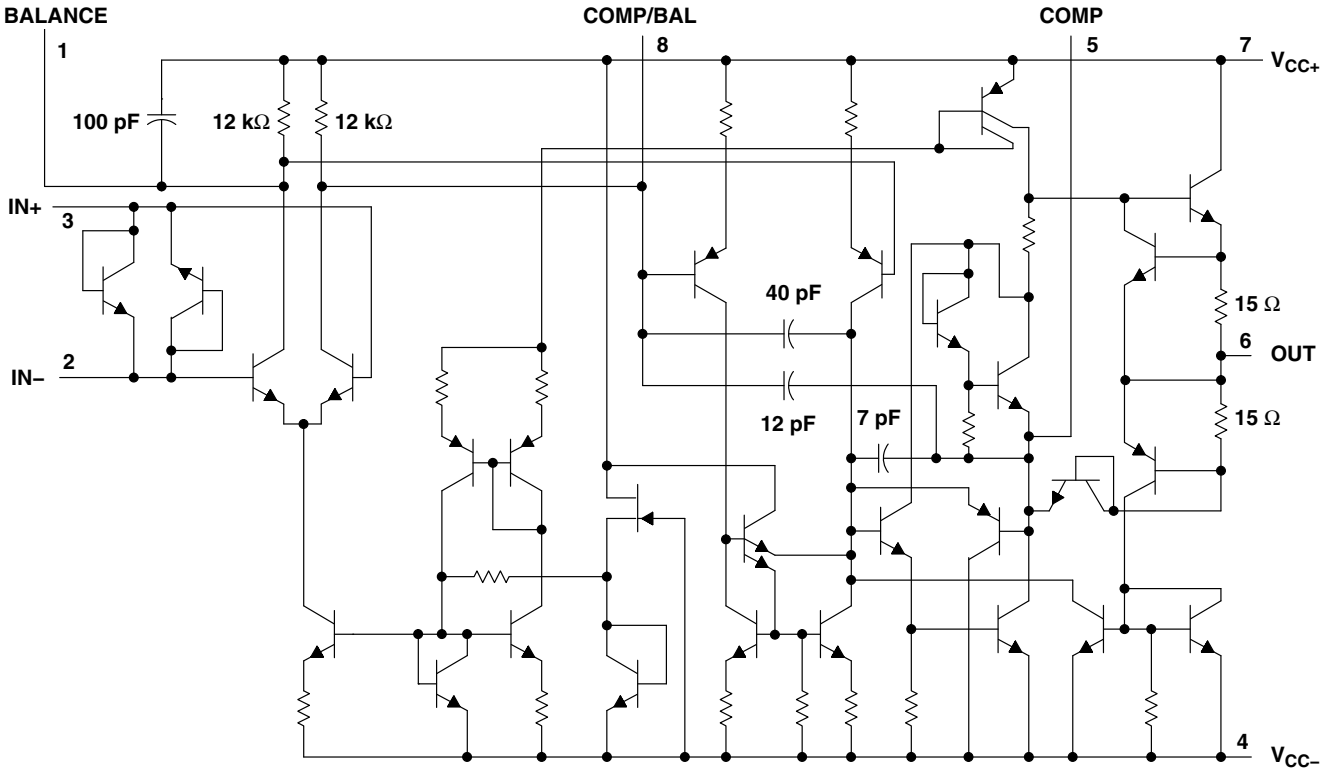
description/ordering information (continued)

ORDERING INFORMATION

T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	4 mV	PDIP (P)	Tube of 50	NE5534P	NE5534P
			Tube of 50	NE5534AP	NE5534AP
		SOIC (D)	Tube of 75	NE5534D	NE5534
			Reel of 2500	NE5534DR	
			Tube of 75	NE5534AD	5534A
			Reel of 2500	NE5534ADR	
		SOP (PS)	Reel of 2000	NE5534PSR	N5534
–40°C to 85°C	4 mV	PDIP (P)	Tube of 50	SA5534P	SA5534P
			Tube of 50	SA5534AP	SA5534AP
		SOIC (D)	Tube of 75	SA5534D	SA5534
			Reel of 2500	SA5534DR	
			Tube of 75	SA5534AD	SA5534A
			Reel of 2500	SA5534ADR	
		SOP (PS)	Tube of 80	SA553APS	SA5534
			Reel of 2000	SA553APSR	

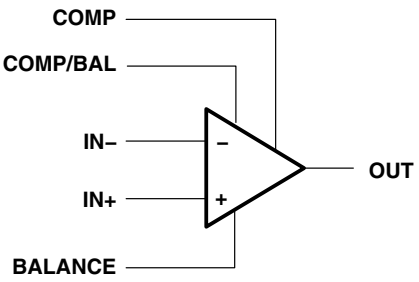
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic

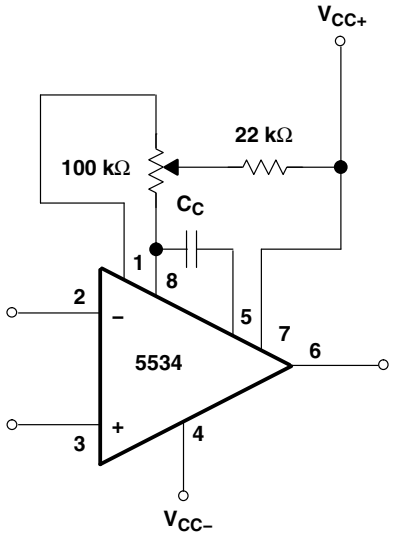


All component values shown are nominal.

symbol



application circuit



Frequency Compensation and Offset-Voltage Nulling Circuit

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1) . . . . . 22 V
V_{CC-} (see Note 1) . . . . . –22 V
Input voltage either input (see Notes 1 and 2) . . . . . V_{CC+}
Input current (see Note 3) . . . . . ±10 mA
Duration of output short circuit (see Note 4) . . . . . Unlimited
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package . . . . . 97°C/W
P package . . . . . 85°C/W
PS package . . . . . 95°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
4. The output may be shorted to ground or to either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
T_A	Operating free-air temperature range	NE5534, NE5534A	0	70	°C
		SA5534, SA5534A	–40	85	

electrical characteristics, $V_{CC}\pm$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		0.5	4	mV
			T_A = Full range			5	
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		20	300	nA
			T_A = Full range			400	
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		500	1500	nA
			T_A = Full range			2000	
V_{ICR}	Common-mode input voltage range			±12	±13		V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	R_L ≥ 600 Ω	$V_{CC\pm}$ = ±15 V	24	26		V
			$V_{CC\pm}$ = ±18 V	30	32		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 600 Ω	T_A = 25°C	25	100		V/mV
			T_A = Full range	15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz	C_C = 0		6		V/mV
			C_C = 22 pF		2.2		
B_{OM}	Maximum-output-swing bandwidth	V_O = ±10 V	C_C = 0		200		kHz
			C_C = 22 pF		95		
		$V_{CC\pm}$ = ±18 V, R_L ≥ 600 Ω,	V_O = ±14 V, C_C = 22 pF		70		
B_1	Unity-gain bandwidth	C_C = 22 pF,	C_L = 100 pF		10		MHz
r_i	Input resistance			30	100		kΩ
z_o	Output impedance	A_{VD} = 30 dB, C_C = 22 pF,	R_L ≥ 600 Ω, f = 10 kHz		0.3		Ω
CMRR	Common-mode rejection ratio	V_O = 0, R_S = 50 Ω	V_{IC} = V_{ICR}min,	70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC+} = ±9 V to ±15 V, V_O = 0	R_S = 50 Ω,	80	100		dB
I_{OS}	Output short-circuit current				38		mA
I_{CC}	Supply current	V_O = 0, No load	T_A = 25°C		4	8	mA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. For NE5534 and NE5534A, full range is 0°C to 70°C. For SA5534 and SA5534A, full range is –40°C to 85°C.

operating characteristics, $V_{CC}\pm = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	NE5534, SA5534	NE5534A, SA5534A			UNIT
			TYP	MIN	TYP	MAX	
SR	Slew rate	$C_C = 0$	13		13		V/μs
		$C_C = 22$ pF	6		6		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 22$ pF, $C_L = 100$ pF	20		20		ns
	Overshoot factor		20		20		%
	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 47$ pF, $C_L = 500$ pF	50		50		ns
	Overshoot factor		35		35		%
V_n	Equivalent input noise voltage	f = 30 Hz	7		5.5	7	nV/√Hz
		f = 1 kHz	4		3.5	4.5	
I_n	Equivalent input noise current	f = 30 Hz	2.5		1.5		pA/√Hz
		f = 1 kHz	0.6		0.4		
$\overline{F}$	Average noise figure	$R_S = 5\ k\Omega$, f = 10 Hz to 20 kHz			0.9		dB

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

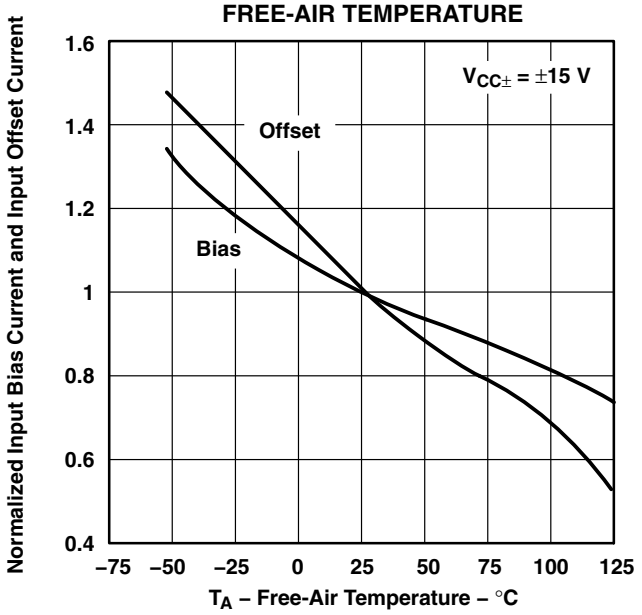


Figure 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

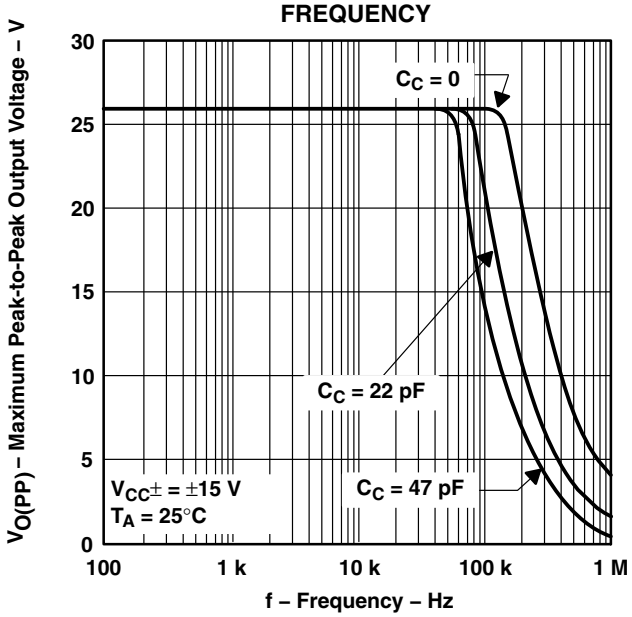


Figure 2

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

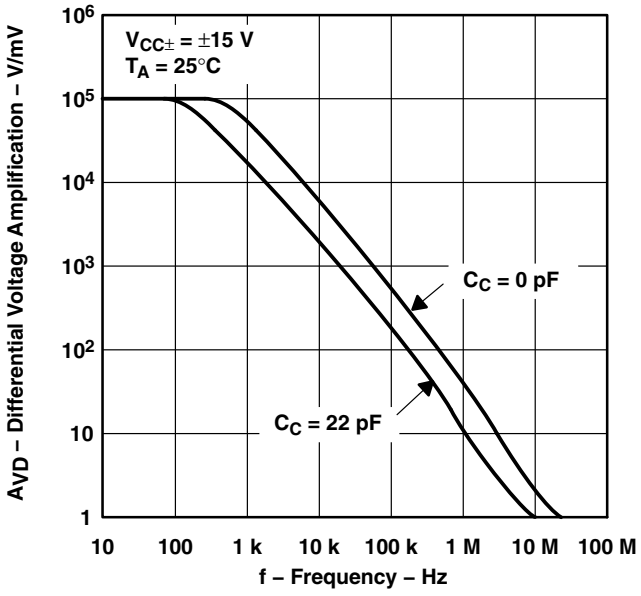


Figure 3

NORMALIZED SLEW RATE AND UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

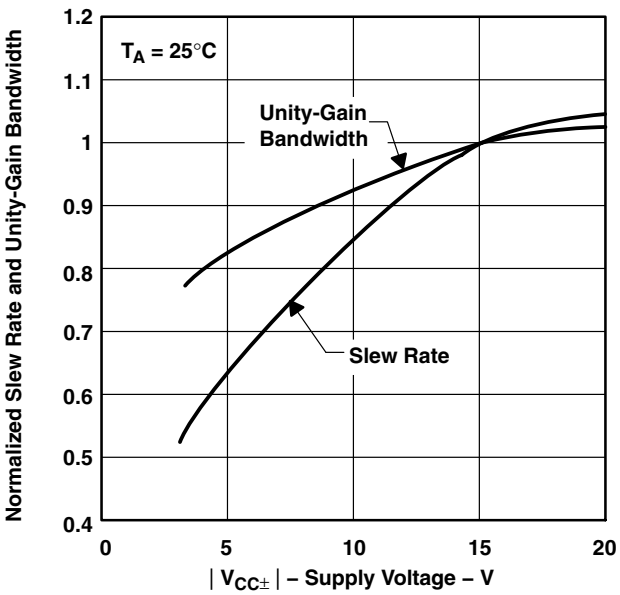


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NORMALIZED SLEW RATE AND UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

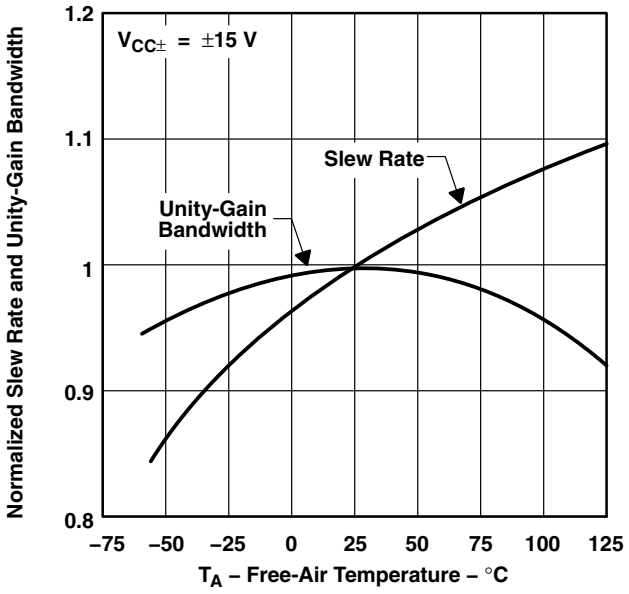


Figure 5

TOTAL HARMONIC DISTORTION vs FREQUENCY

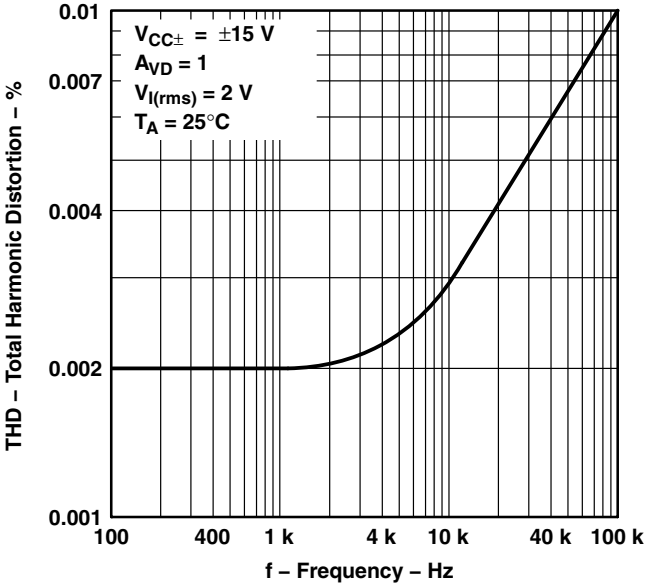


Figure 6

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

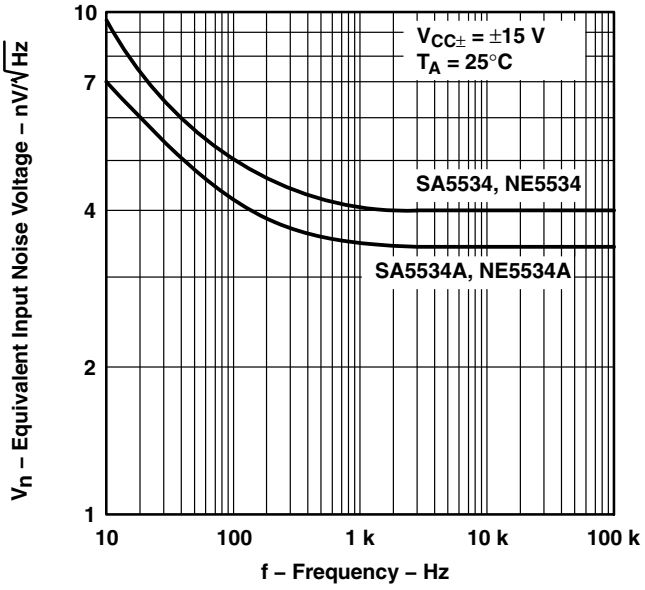


Figure 7

EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

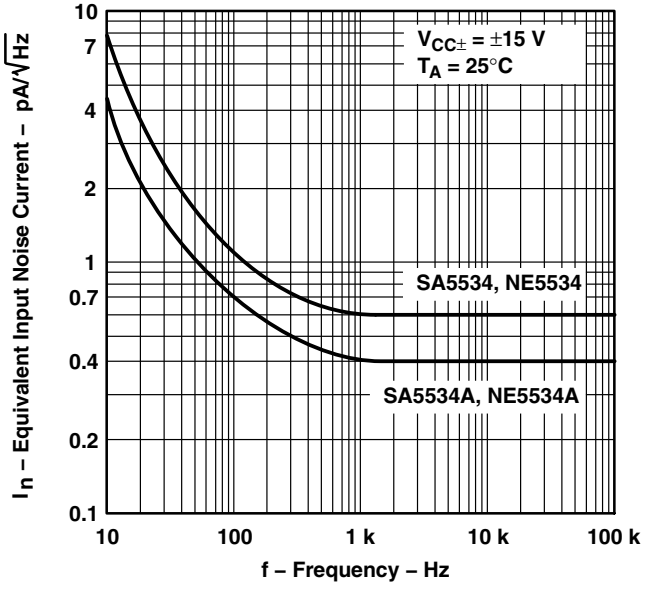


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TOTAL EQUIVALENT INPUT NOISE VOLTAGE vs SOURCE RESISTANCE

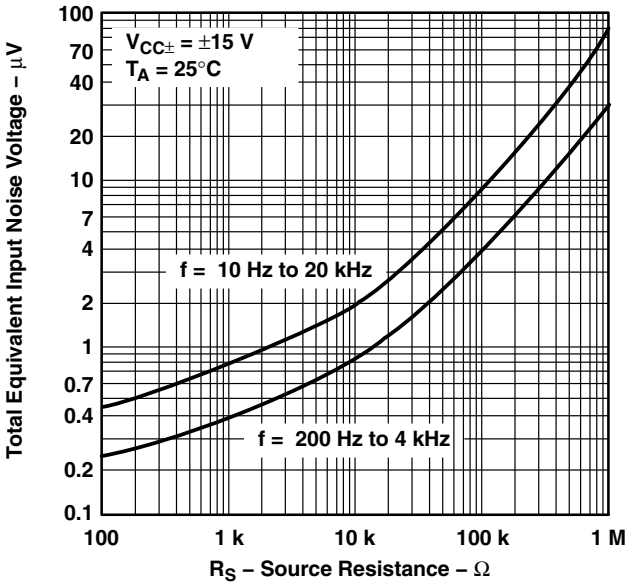


Figure 9

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
NE5534AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534AJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
NE5534AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg
NE5534APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg
NE5534D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
NE5534IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
NE5534P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg
NE5534PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg
SA5534AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
SA5534ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg
SA5534APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg
SA5534D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SA5534P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg
SA5534PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg
SA5534PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SA5534PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SA5534PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate inf
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical an
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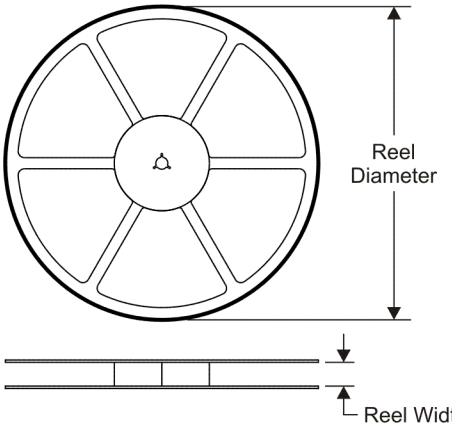
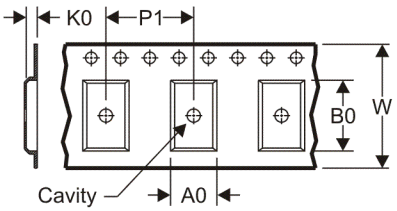
TAPE AND REEL INFORMATION

REEL DIMENSIONS

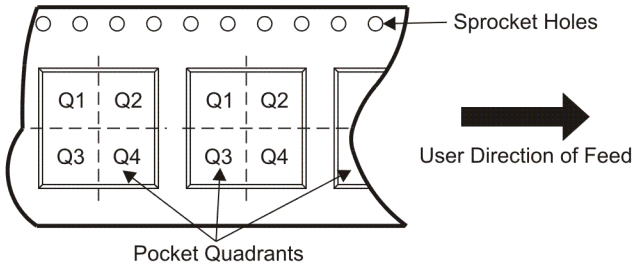


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

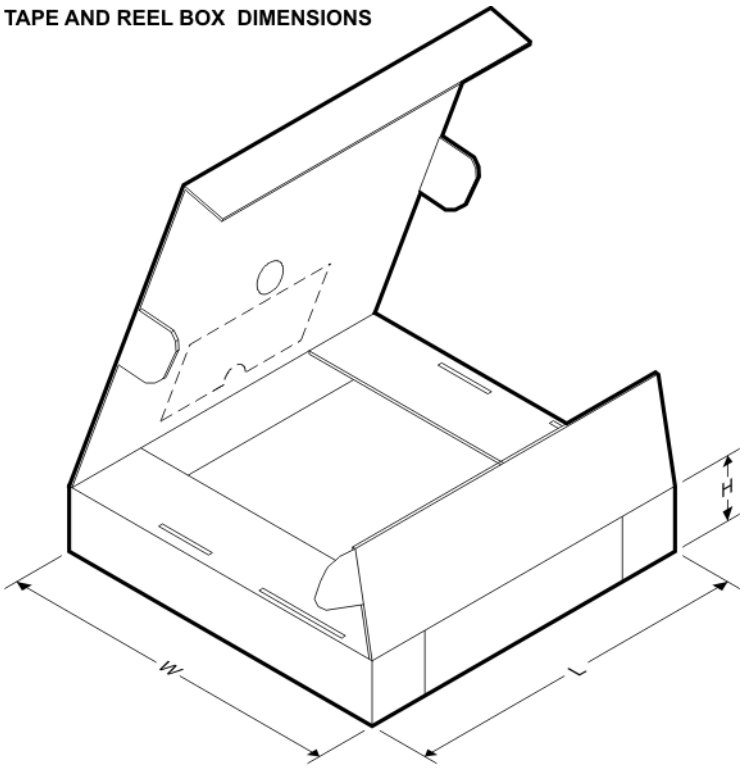
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NE5534ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5534DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5534ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5534DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5534PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

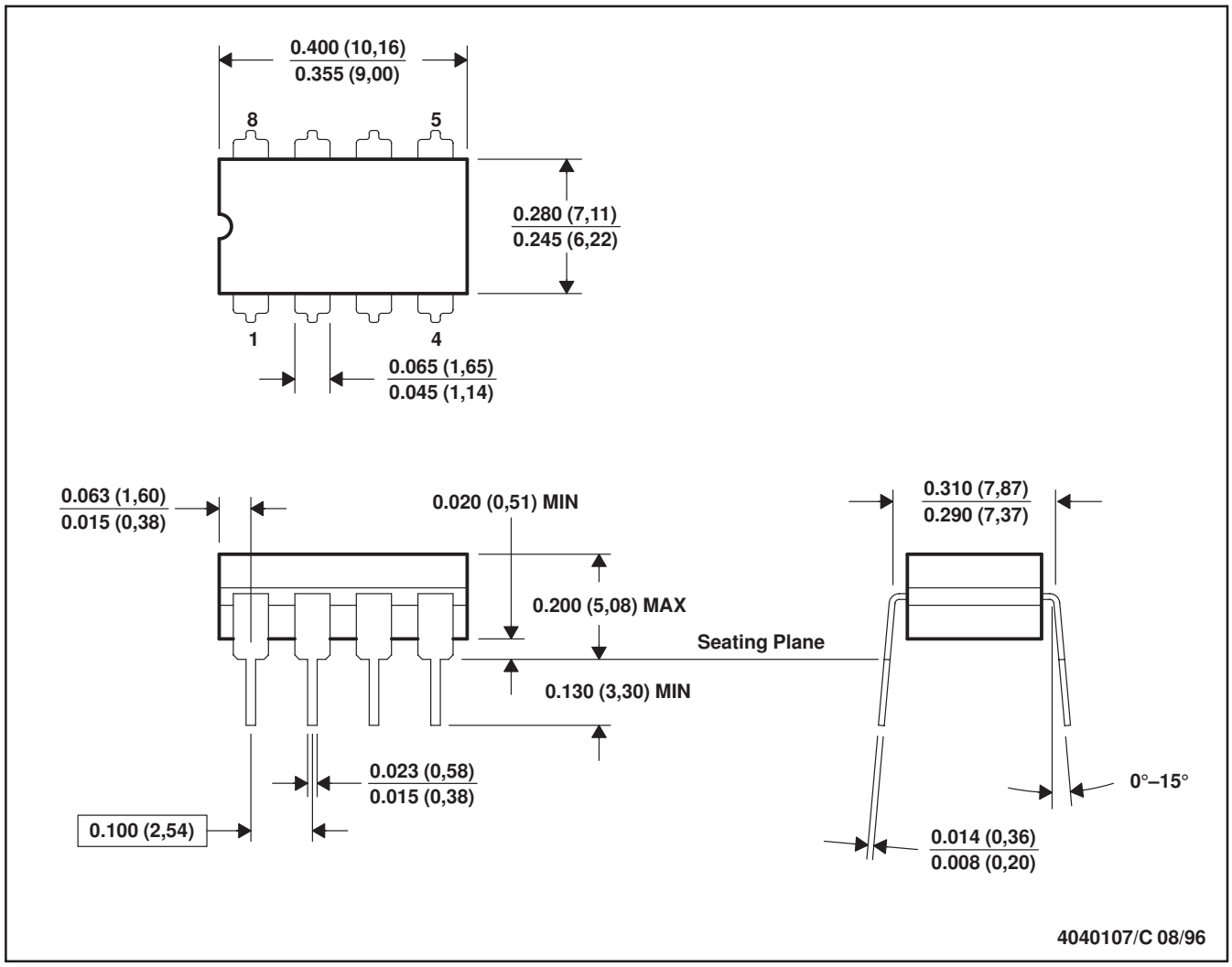


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NE5534ADR	SOIC	D	8	2500	340.5	338.1	20.6
NE5534DR	SOIC	D	8	2500	340.5	338.1	20.6
SA5534ADR	SOIC	D	8	2500	340.5	338.1	20.6
SA5534DR	SOIC	D	8	2500	340.5	338.1	20.6
SA5534PSR	SO	PS	8	2000	346.0	346.0	33.0

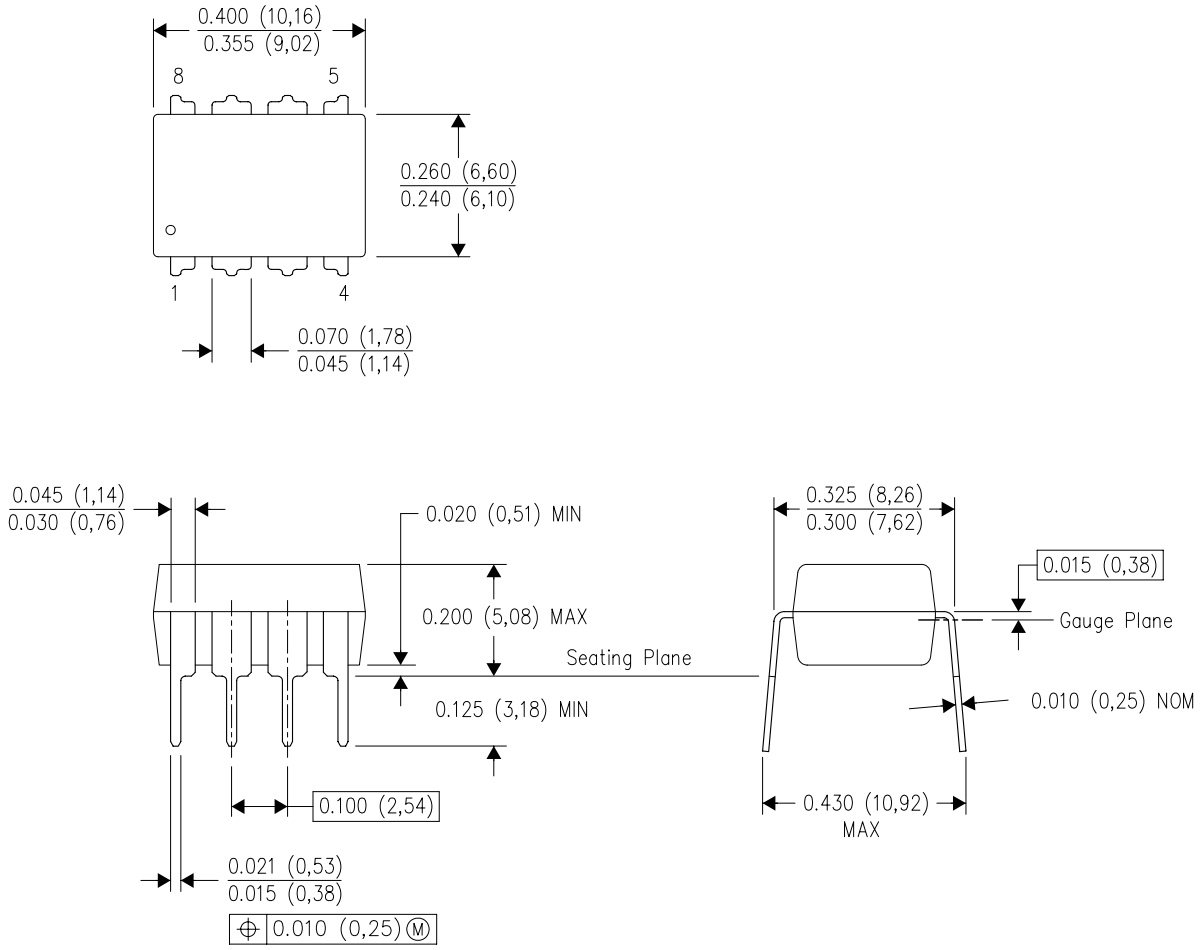
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



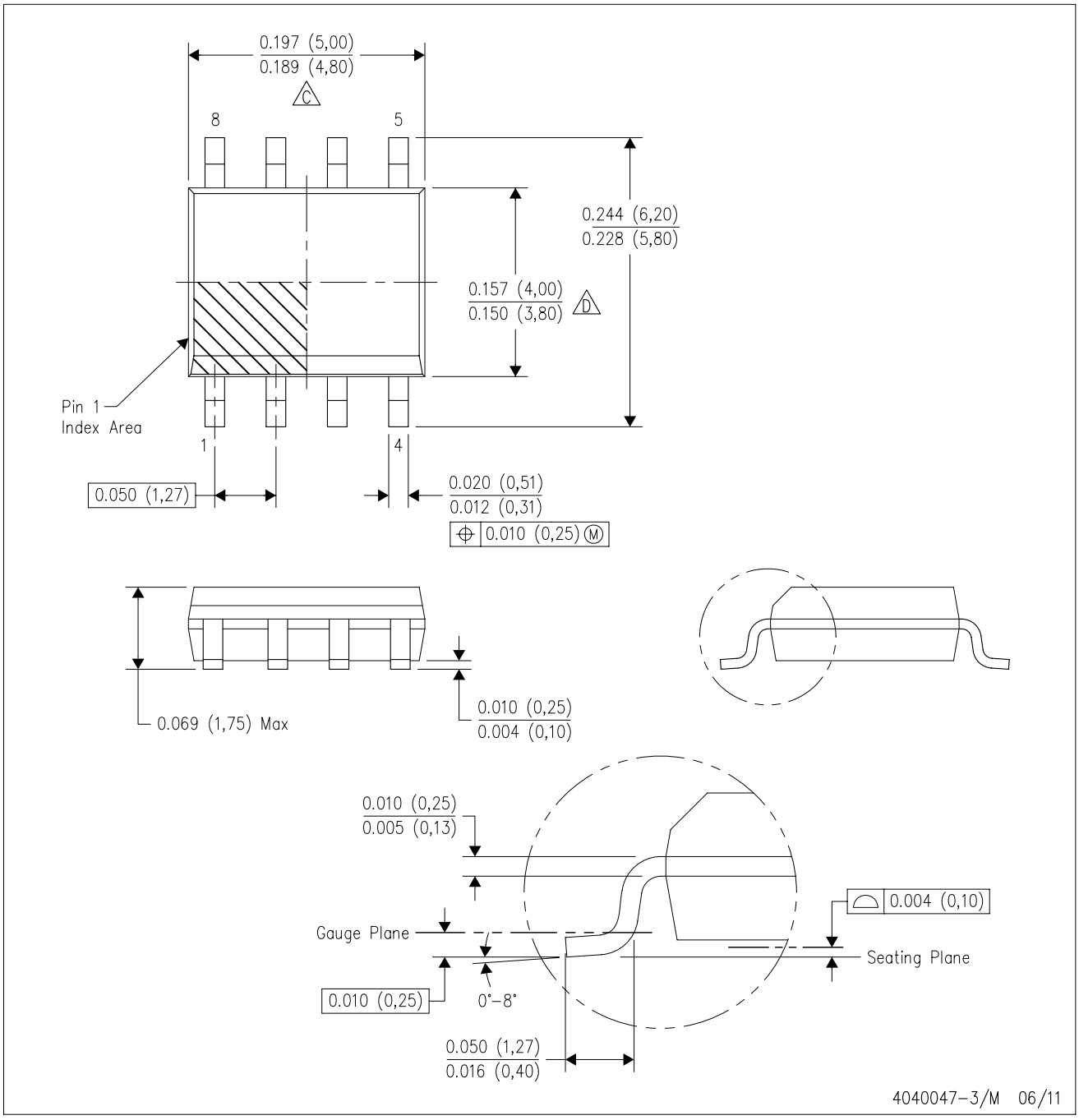
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



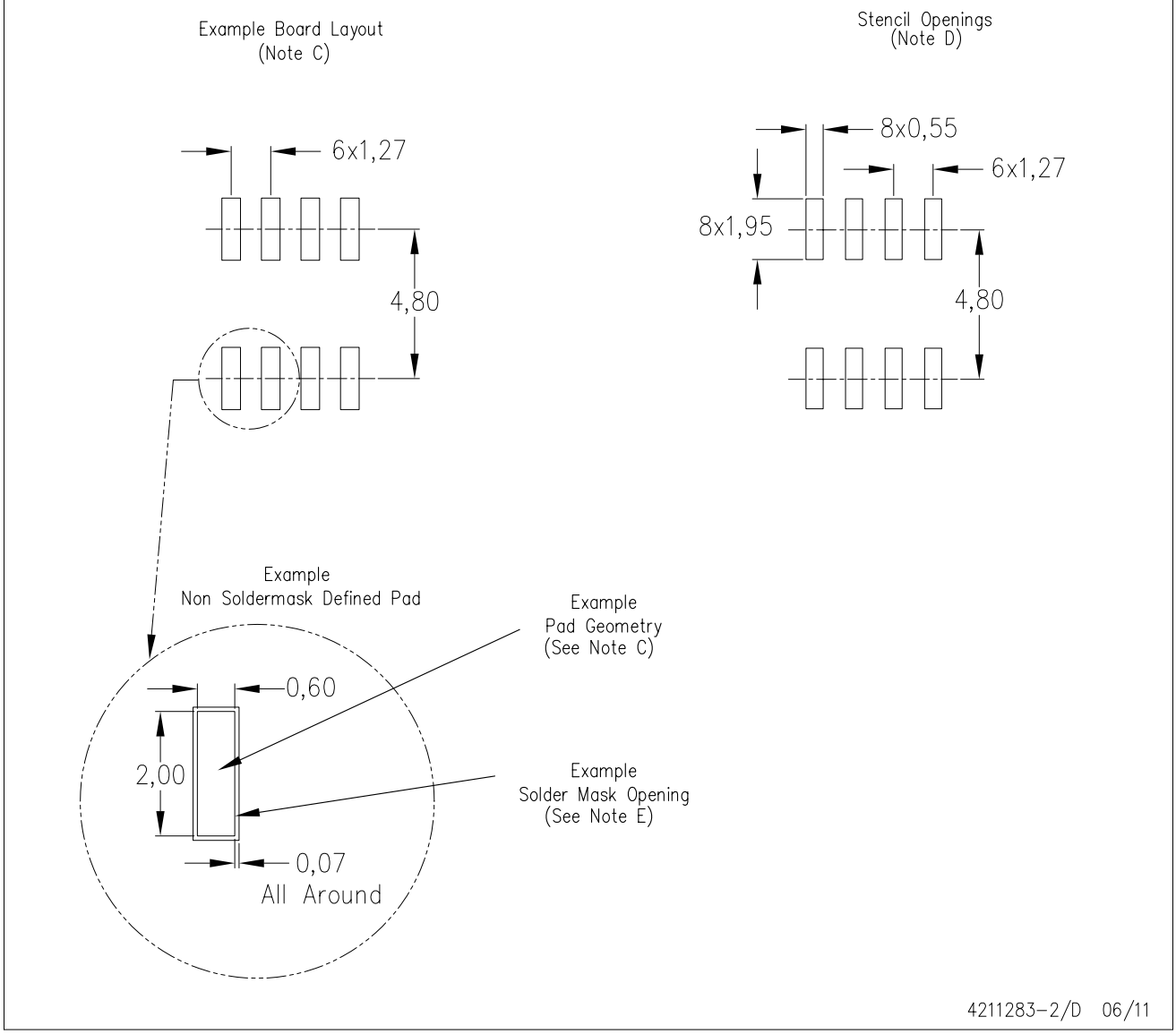
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

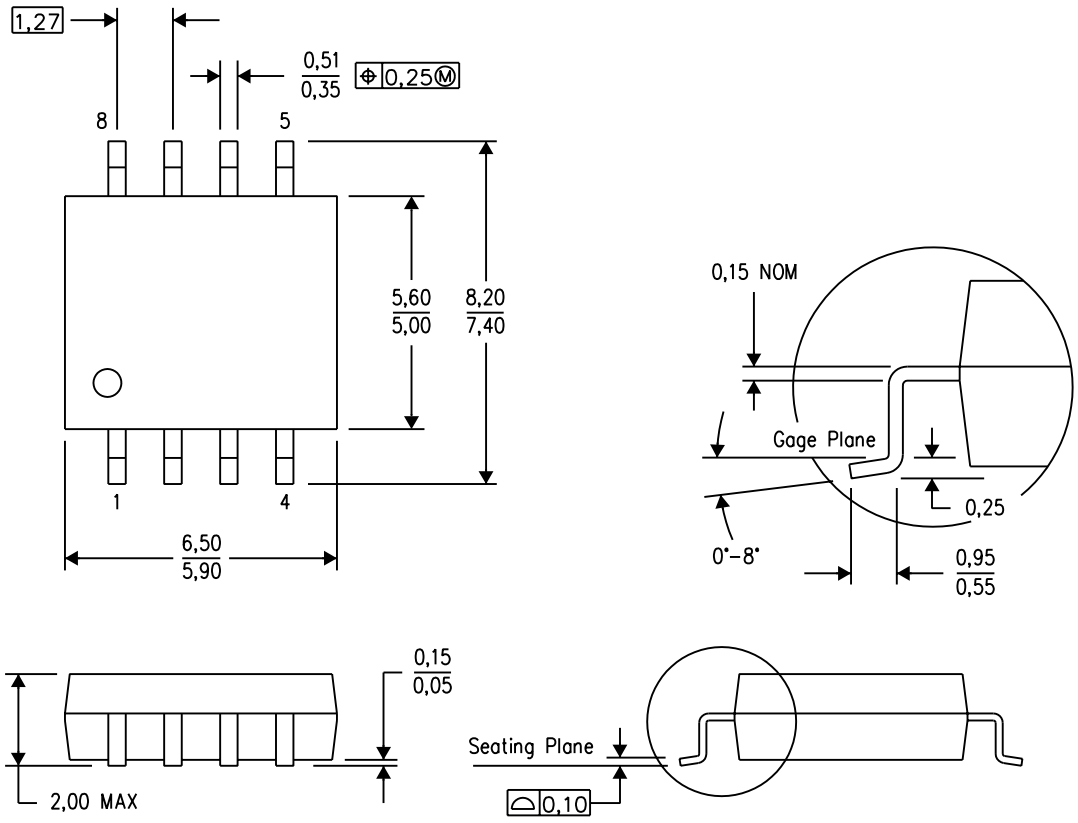
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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